UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/589,966	06/08/2000	Michael J. Demler	ANTR-01016US1	1467

23910 7590 02/13/2003

FLIESLER DUBB MEYER & LOVEJOY, LLP
FOUR EMBARCADERO CENTER
SUITE 400
SAN FRANCISCO, CA 94111

EXAMINER
PHAN, THAI Q

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 02/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/589,966	Applicant(s) Michael J. Demler
	Examiner Thai Phan	Art Unit 2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jun 8, 2000*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-14* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *5 and 6*
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is response to patent application S/N: 09/589,966. Claims 1-14 are pending in this Office Action.

Drawings

1. The drawings are objected by the draftsperson's patent drawing review (see Form PTO 948 enclosed). The examiner suggests applicant to remove the legend "Antrim Design System Confidential" at the bottom of the drawings in the present patent application.

Information Disclosure Statement

2. The information disclosure statements filed on Dec. 27, 2000 and Apr. 09, 2001 have been considered and placed in the record.

Claim Objections

3. Claim 4 is objected to under 37 CFR 1.75© as being in improper form because a multiple dependent claim 4 on any claims 1-3. See MPEP § 608.01(n). However, the claim has been treated on the merits.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 12 recites the limitation "The mixed signal synthesizer" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 1-4, 7-9, and 12-14 are rejected under 35 U.S.C. 103(a) as being obvious over Spruiell et al., US patent no. 6,356,796 B1 in view of Barford et al., US patent no. 5,946,482.

The applied reference has a common assignee or at least one common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104,

together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

As per claim 1, Spruiell discloses method and system for simulating, verifying and characterizing device for circuit design with feature limitations as substantially similar to the claimed invention (Abstract and Summary of the Invention). According to Spruiell, the method of making a plan for circuit synthesis includes steps and means for determining circuit design comprising at least one set of circuit elements (col. 1, lines 43-59, for example), means for identifying a set of parameters for construction of the circuit elements (col. 5, Characterization Plans), means for simulating operation of the circuit at points defined by design parameters or design parameter values defined by user (col. 3, lines 23-33, col. 5, lines 5-50) for characterization, means for consolidating the simulation results for the design, and storing means for storing the consolidated results of the simulation in a behavioral model of the plan (col. 3, lines 54-62, col. 5, lines 5-50, col. 8, lines 14-21). Spruiell does not explicitly disclose set of points, each point defined by varying at least one of the parameters in the design simulation process as claimed. Such feature is well-known in the art. In fact, Barford teaches method and system for designing and simulating circuit using circuit design parameters to characterize design device operation (Summary of the Invention). The simulator uses a set of points, each set point being defined by varying design parameters to fit with design behavior (col. 4, lines 1-18, col. 5,

lines 15-56, col. 6, lines 32-51, for example). Such circuit simulation could provide an effective way to simulate and characterize the design behaviors in circuit synthesis (col. 1, Field of the Invention, col. 3, lines 32-45).

This would motivate practitioner in the art at the time of the invention to combine Barford teaching of simulating a design on a set of points each defined by varying design parameters to circuit design plans as disclosed in Spruiell to effectively simulate the design and reduce the complexity of the design on a portion of the circuit or effect due to various parts of the design as suggested in Barford, col. 1, lines 10-33, col. 3, lines 32-45.

As per claim 2, Spruiell discloses storing simulation results in storage means. The store formats include tabular form corresponding to each simulation process on a set of points as claimed (Fig. 2).

As per claim 3, Barford teaches polynomial fitted transfer equation over a design parameter values (col. 3, line 46 to col. 4, line 18).

As per claim 4, Spruiell and Barford disclose analog design as claimed.

As per claim 7, Spruiell discloses method and system for simulating, verifying and characterizing device for circuit design with feature limitations as substantially similar to the claimed invention (Abstract and Summary of the Invention). According to Spruiell, the method of making a plan for circuit synthesis includes steps and means for determining circuit design comprising at least one set of circuit elements (col. 1, lines 43-59, for example), means for identifying a set of parameters for construction of the circuit elements (col. 5, Characterization Plans), means for simulating operation of the circuit at points defined by design parameters or

design parameter values defined by user (col. 3, lines 23-33, col. 5, lines 5-50) for characterization, means for consolidating the simulation results for the design, and storing means for storing the consolidated results of the simulation in a behavioral model of the plan (col. 3, lines 54-62, col. 5, lines 5-50, col. 8, lines 14-21). Spruiell does not explicitly disclose set of points, each point defined by varying at least one of the parameters in the design simulation process , and fitting a polynomial curve to a result of the circuit simulation at each of the set of points as claimed. Such features are well-known in the art. In fact, Barford teaches method and system for designing and simulating circuit using circuit design parameters to characterize design device operation (Summary of the Invention). The simulator uses a set of points, each set point being defined by varying design parameters to fit with design behavior (col. 4, lines 1-18, col. 5, lines 15-56, col. 6, lines 32-51, for example). Barford also teaches polynomial fitted transfer equation over a design parameter values (col. 3, line 46 to col. 4, line 18). Such particular circuit simulation could provide an effective way to simulate and characterize the design behaviors in circuit synthesis (col. 1, Field of the Invention, col. 3, lines 32-45).

This would motivate practitioner in the art at the time of the invention to combine Barford teaching of simulating a design on a set of points each defined by varying design parameters to circuit design plans as disclosed in Spruiell to effectively simulate the design and reduce the complexity of the design on a portion of the circuit or effect due to various parts of the design as suggested in Barford, col. 1, lines 10-33, col. 3, lines 32-45.

As per claim 8, Spruiell discloses setting parameters to a fixed value (col. 5, Characterization and Synthesis Plans), setting values for other parameters for the complete

design (col. 5, col. 6), simulating the circuit design to produce a result (col. 5), varying the parameter information in parameter design space to optimize the design (cols. 4-5), and repeating the steps of varying and simulating for a predetermined number of iteration to optimize the design.

As per claim 9, Barford discloses repeating step of simulating and fitting to produce simulation result, and selecting an optimized circuit solution from the set of simulation data points (cols. 3, 6).

As per claim 12, Spruiell discloses netlists which would include non-sized ones for the design optimization process, design topology for the design and placement, synthesis model, etc. as claimed (Fig. 1, cols. 3-4, for example).

As per claim 13, Spruiell discloses synthesis engine including a plurality of synthesis plans (Fig. 1, Summary of the Invention), and tool selecting means for selecting design tools for the synthesis plan.

As per claim 14, Spruiell discloses a plurality of tools for design optimization, such tools includes simulator, plan optimizer, etc. (Fig. 1, col. 5, lines 17-30).

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

9. Claims 5, 6 and 10-11 are rejected under 35 U.S.C. 102(e) as being by Spruiell et al., patent no. 6,356,796 B1.

As per claim 5, Spruiell anticipates method and system for simulating circuit with feature limitations identical to the claimed invention (Abstract and Summary of the Invention). According to Spruiell, the simulation method includes steps of selecting a plan for a circuit to be designed (col. 1, lines 35-42), providing the selected plan and a set of performance requirements to a synthesis engine (col. 2, line 62 to col. 3, line 48, for example), executing the plan for the

simulation and design, and retrieving results of the execution plan (col. 3, line 49 to col. 5, line 42, col. 8, lines 3-12).

As per claim 6, Spruiell anticipates results including sized netlist for specific design, simulation scripts, etc. (Figs. 1, 2, col. 5, lines 16-25, col. 8, lines 3-12).

As per claim 10, Spruiell anticipates circuit design and synthesis engine configured to determine an optimized and produces a sized netlist on a plan having a circuit design and parameters for optimizing the circuit (Figs. 1, 2, col. 1, lines 35-42, col. 2, line 62 to col. 3, line 48, col. 3, line 39 to col. 5, line 42, and col. 8, lines 3-12).

As per claim 11, Spruiell anticipates synthesis plan library having a set of synthesis plans for the circuit under design (Fig. 1, col. 5, lines 17-26), each synthesis plan having a circuit design and a set of design parameters and values relating to physical characteristics of the circuit elements, an user interface configured to allow user to select a synthesis plan from the library and input the plan and a set of design parameters relating to performance characteristics to the synthesis engine (Fig. 1, Summary of the Invention, col. 2, line 62 to col. 4, line 23, for example).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 4,791,593, issued to Hennion, Bernard, on Dec. 1988
2. US patent no. 5,535,223, issued to Horstmann et al., on July 1996
3. US patent no. 5,838,947, issued to Sarin, Harish, on Nov. 1998

4. US patent no. 6,308,300 B1, issued to Bushnell et al., on Oct. 2001

5. US patent no. 6,499,129 B1, issued to Srinivasan et al., on Dec. 2002

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239, (for formal communications intended for entry)

Or:

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

February 9, 2003

Thaphan
Patent Examiner
AU 2123